Claims

1. A method of forming an isolation in a semiconductor substrate comprising:

(a) providing a semiconductor substrate;

(b) forming a plurality of adjacent trenches in said semiconductor substrate leaving adjacent segments of said semiconductor substrate between each of said adjacent trenches;

(c) depositing a barrier layer in said plurality of adjacent trenches;

(d) removing a portion of said barrier layer in each of said plurality of adjacent trenches to expose portions of said adjacent segments of said semiconductor substrate,

(e) merging said exposed portions of said adjacent segments of said semiconductor substrate to form a self-aligned shallow trench isolation.

2. The method of claim 1 wherein step (a) comprises providing a silicon substrate having a pad dielectric layer thereover a surface of said silicon substrate.

3. The method of claim 2 wherein said pad dielectric layer comprises a pad oxide layer followed by a pad nitride layer.

4. The method of claim 1 wherein step (b) comprises etching a plurality of adjacent vertical deep trenches in said semiconductor substrate leaving said adjacent segments of said semiconductor substrate between each of said plurality of adjacent vertical deep trenches.

5. The method of claim 1 wherein step (c) comprises depositing an oxidation barrier layer in said plurality of adjacent trenches.

6. The method of claim 1 wherein step (e) comprises merging said exposed portions of said adjacent segments of said semiconductor substrate by oxidation to form a self-aligned thermal oxide shallow trench isolation.

7. The method of claim 1 further including after step (e) the steps comprising:

(f) removing remaining portions of said barrier layer in said plurality of adjacent trenches;

(g) forming a deep trench capacitor within said plurality of adjacent trenches; and

(h) forming a vertical transistor within said plurality of adjacent trenches to form a memory cell.

8. A method of forming isolations in a semiconductor substrate comprising:

(a) providing a silicon substrate;

(b) forming a plurality of adjacent trenches leaving adjacent segments of said silicon substrate between each of said plurality of adjacent trenches;

(c) depositing an oxidation barrier layer in said plurality of adjacent trenches;

(d) recessing a portion of said oxidation barrier layer in each of said plurality of adjacent trenches to expose at least a portion of said adjacent segments of said silicon substrate;

(e) etching said exposed portions of said adjacent segments of said silicon substrate to form a plurality of thin sections of said exposed adjacent segments of said silicon substrate between each of said plurality of adjacent trenches; and

(f) merging said thin sections of said exposed adjacent segments of said silicon substrate at least along a first row of selected ones of said plurality of adjacent trenches to form a self-aligned shallow trench isolation.

9. The method of claim 8 wherein step (a) further comprises depositing a layer of pad oxide thereover said silicon substrate to a thickness ranging from about 1 to about 10 nm.

10. The method of claim 9 wherein step (a) further comprises depositing a layer of pad nitride thereover said layer of pad oxide to a thickness ranging from about 50 to about 500 nm.

11. The method of claim 8 wherein step (b) comprises etching said plurality of adjacent trenches to a depth ranging from about 250 nm to about 10μm.

12. The method of claim 8 wherein step (c) comprises depositing said oxidation barrier layer to at least conformally coat a sidewall and a bottom surface of said plurality of adjacent trenches.

13. The method of claim 8 wherein step (c) comprises depositing an oxidation barrier layer of silicon nitride having a thickness ranging from about 3nm to about 30nm.

14. The method of claim 8 wherein said step (d) of recessing said portion of said oxidation barrier layer comprises:

depositing a photoresist within said plurality of adjacent trenches to at least fill empty portions of said plurality of adjacent trenches;

determining a desired depth in said photoresist to recess said oxidation barrier layer;

etching said photoresist and said oxidation barrier layer stopping at said desired depth in said photoresist thereby recessing said oxidation barrier layer to said

desired depth and exposing said portions of said adjacent segments of silicon substrate in a top portion of said plurality of adjacent trenches.

15. The method of claim 12 wherein step (d) comprises recessing said oxidation barrier layer to a depth ranging from about 20nm to about 2000nm within said plurality of adjacent trenches.
recessing a portion of said oxidation barrier layer in each of said plurality of adjacent trenches to expose at least a portion of said adjacent segments of said silicon substrate.

16. The method of claim 8 wherein step (e) said etched plurality of thin sections of said exposed adjacent segments of said silicon substrate have a diameter ranging from about 1/5 to about 1/2 that of an original diameter of said exposed portions of said adjacent segments of said silicon substrate.

17. The method of claim 8 wherein step (e) comprises etching said exposed portions of said adjacent segments of said silicon substrate using an etchant which selectively removes only said silicon substrate to form said plurality of thin sections of said exposed adjacent segments of said silicon substrate.

18. The method of claim 17 wherein said etchant comprises an etchant selected from the group consisting of a chlorine-containing etchant, KOH, and NH_4OH.

19. The method of claim 8 wherein step (f) comprises oxidizing said thin sections of said exposed adjacent segments of said silicon substrate thereby merging together selected ones of said thin sections of adjacent segments of said silicon substrate at least along said first row of said selected ones of said plurality of adjacent trenches to form a self-aligned silicon dioxide shallow trench isolation.

20. The method of claim 19 wherein said thin sections of said exposed adjacent segments of said silicon substrate are oxidized using a local oxidation of silicon.

21. An isolation structure in a semiconductor substrate comprising:

a semiconductor substrate;

a plurality of adjacent trenches in said semiconductor substrate; and

a self-aligned isolation structure in upper portions of selected ones of said plurality of trenches, said isolation structure being merged portions of said semiconductor substrate along at least a first row of said selected ones of said plurality of adjacent trenches, said merged portions of said semiconductor substrate being aligned as-formed to edges of said plurality of adjacent trenches,

wherein said self-aligned isolation structure isolates a first region of said semiconductor substrate from a second region of said semiconductor substrate.

22. The apparatus of claim 21 wherein said semiconductor substrate comprises a silicon substrate.

23. The apparatus of claim 21 further including a pad dielectric layer thereover a surface of said semiconductor substrate.

24. The apparatus of claim 23 wherein said pad dielectric layer comprises a pad oxide layer followed by a pad nitride layer.

25. The apparatus of claim 24 wherein said pad oxide layer has a thickness ranging from about 1 nm to about 10 nm.

26. The apparatus of claim 24 wherein said pad nitride layer has a thickness ranging from about 50 nm to about 500 nm.

27. The apparatus of claim 21 wherein said plurality of adjacent trenches have depths ranging from about 250 nm to about 10μm.

28. The apparatus of claim 21 wherein said self-aligned isolation structure comprises a thermal oxide region existing along said at least first row of selected ones of said plurality of adjacent trenches.

29. The apparatus of claim 28 wherein said semiconductor substrate comprises a silicon substrate and said thermal oxide region comprises a thermal silicon dioxide region existing along said at least first row of selected ones of said plurality of adjacent trenches.

30. An isolation structure in a semiconductor substrate comprising:

a silicon substrate having a layer of pad oxide disposed thereover said silicon substrate and a layer of pad nitride disposed thereover said pad oxide;

a plurality of adjacent trenches traversing through said pad oxide, said pad nitride, and stopping in said silicon substrate; and

a self-aligned, thermal oxide isolation structure in upper portions of said plurality of adjacent trenches, said thermal oxide isolation structure being oxidized portions of said semiconductor substrate merged along at least a first row of selected ones of said plurality of adjacent trenches in said upper portions of said trenches, said oxidized portions of said semiconductor substrate being aligned as-formed to edges of said plurality of adjacent trenches,

wherein said thermal oxide isolation structure isolates a first region of said semiconductor substrate from a second region of said semiconductor substrate.